

Full Receiver Specifications

Amplifier Circuit:

- Gain: 4dB – 68 dB, 1dB increments
- 3.5 dB NF at maximum gain
- IP3 > 42 dB
- Controlled via USB or parallel interface
- Blanking isolation with inverse blocking switch

Sampling Circuit:

- Sample Rate: ~100 MSPS at 16 bit
- Output Format after digital decimation: 64 bit IQ pair
- Information content may be Bandwidth dependent
- Scan Frequency range: 6 MHz -> 500 MHz
- 100 dB SFDR
- 13 dBm Full Scale Input Range
- Output Bandwidth range: 1kHz -> 5 MHz

Mixing:

- Patented method occurs digitally via PhaseLock technology

Required Inputs:

- 10 MHz System Clock
- Local Synthesizer Oscillator
- Trigger with blanking encode
- RF Signal from Coil Preamplifiers

Computer System:

- Dual AMD or Intel multi core Server processors
- 16 GB RAM
- Linux installation
- 1 TB RAID

Form Factor:

- 19 inch rack Mount
Height depends on number of channels

